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Latency Improved Hybrid Majority and Minority Designs for Image Processing Applications

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ABSTRACT The increasing amount of circuit density possible in CMOS technology has the consequence of also increasing the power consumption of circuits using the technology. One possible method of offsetting these increased power demands is to use approximate computing designs in circuits where complete accuracy is not a strict requirement. These circuits use fewer logic gates which reduces power consumption at the cost of accuracy. Another possible method for reducing power consumption is to use an emerging nanotechnology which is already low power in nature. Combining approximate computing with an emerging nanotechnology has the potential to further cut power consumption. Unfortunately, existing approximate computing circuits were designed using standard logic gates found in CMOS technology which in turn can limit their effectiveness when implemented with the majority based logic used by some emerging nanotechnologies. For that reason, I propose designs of approximate arithmetic units which are specifically designed for use in majority logic based technologies. The current proposed design aims to initiate the model and its design scenario for each set of applications which I intended to work on. Our design proposes a majority gate based on 2 XOR and 2 OR gates which utilizes the design and its model for the design of 4 bit adder and with an existing case in 32nm CMOS technology as a back end design and front end design with 4 bit Adder.

Index Terms - majority logic, approximate adder, and approximate multiplier, complement bits, approximate compressor and image processing.

INTRODUCTION: The increasing demand for portable products further necessitates the requirement of low power circuits. The changing market demands in favor of portability and modularity of different products to ease out daily life and to enhance the comfort level play a major role in compacting different functionalities. On the other hand the advancements in the battery technology lag the technological advancement in the circuit integration capabilities. The power per unit volume in the batteries has increased many-fold but to fulfill the ever-increasing demand these advances become insufficient. Frequent battery replacement is not feasible because of different limitations the working environment. Especially for health care products that are implanted into human body itis not feasible to operate the

patent for battery replacement. With the ever increase of the products in daily life globally the environmentalists have expressed their worries about the power dissipation from the electronic products. They consider this issue in two fold. Firstly the direct heat dissipated and secondly the heat dissipated by the electronic appliances installed to remove the heat from the working ecosystem to the environment. Due to above-discussed factors it is very essential to integrate and implement the desired functionality using power aware circuits. Traditionally many low power technologies have been proposed and are used to satisfy the power requirements. And there is no single technique which can address the power issues single handedly. Different techniques are to be used simultaneously for the same. In pursuance of the same some concepts from other science domains are also borrowed into VLSI design domain for achieving the desired power constraints. Adiabatic Logic is one such concept that has been adopted from classical thermo-mechanical systems. The idea of zero heat exchange of the system with the environment has motivated the circuit designers to try and implement this while designing the circuit configurations and topologies for different functionalities.

MAJORITY GATES 2BIT DESIGN: Various methods have been proposed for designing ap-proximate circuits which can be categorized into two broad methodologies. The first methodology is based on voltage over scaling (VOS) such as algorithmic noise tolerance (ANT) [6] and significance driven computation (SDC) [7] for modifying or limiting the resultant errors. The second methodology approximates fundamental logic functions at the circuit-level such as a variety of approximate adder realizations [1], [8], [9].As a basic building block in most DSP systems, the multi-pliers is typically located on the critical path of such systems, so it contributes significantly to the system‘s total power consumption and propagation delay, which greatly motivates the need for fast multiplier designs. A fast multiplication operation is usually performed in three steps, including partial product (PP) generation, PP reduction using a carry-save adder(CSA) tree and a fast carry propagation adder (CPA) for the final computation of the product [10]. Most specifically, the PP reduction circuit is crucial in determining the design complexity, latency and power consumption of a multiplier. Hence, improving the performance and energy efficiency of the PP reduction circuit using appropriate arithmetic blocks, such as compressors, can directly improve the performance and energy efficiency of a fast multiplier [5], [11]. Basically, using compressors can reduce energy dissipation by decreasing the number of PP stages in a multiplier. Optimized designs of accurate 4-2 compressors have been proposed in [10], [12]. In addition, several approximate compressors have recently been presented in the literature [13], [14].These approximate compressors have typically been realized using Complementary Metal-Oxide-Semiconductor (CMOS) AND-OR gates that increase the design complexity and XOR gates that increase the overall switching activity. On the other hand, as I approach the physical limit of CMOS devices, an urgent need arises for a potential alternative or complementary computing technology. Among others, spintronic devices [15] have shown significant promise over the past decade because of their non-volatility, zero leakage current, high integration density, low standby power, and Back End of Line fabrication with the

CMOS technology [16]. In this context, different accurate and approximate circuit designs have been presented [17]–[20]. Additionally, leveraging majority logic in nano scale technologies can bring even higher performance and energy efficiency compared to conventional implementations of arithmetic circuits.

EXISITNG DESIGN

IMPLEMENTATION OF MAJORITY GATE WITH XOR AND ITS 16 BIT MULTIPLIER DESIGN

The reduction of feature size and the increase of integration density have pushed CMOS technology to fast approaching its limits; power consumption is still one of the main obstacles in the development of integrated circuits. Approximate computing provides a new approach for low power design at the cost of accuracy loss, while improving performance for error-tolerant applications, including those for digital signal processor (DSP), machine learning and pattern recognition [1-2].Emerging nanotechnologies have been investigated as promising alternatives to CMOS. These nanotechnologies such as quantum-dot cellular automata (QCA) [3], Nano-magnetic logic (NML) [4], and spin-wave devices (SWD) [5], are mostly based on majority logic (ML), so substantially different from conventional Boolean logic. The majority gate performs a multi-input logic operation (Fig. 1); the logic expression for the 3-input majority gate (or voter, MV) is given by

$$F = M(A, B, C) = AB + BC + AC$$

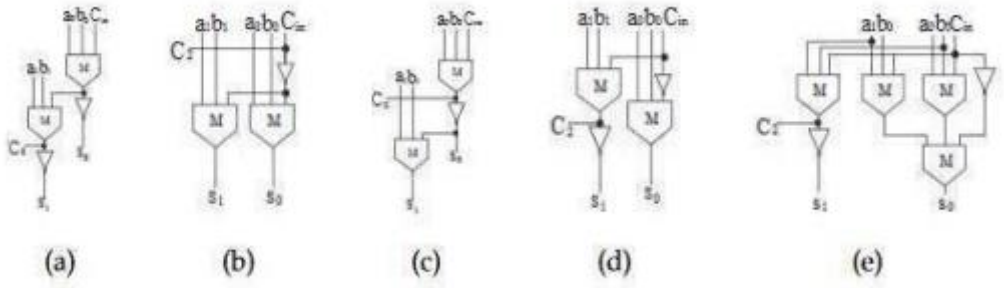

Fig 1 Carry out Sum

where the 3-input majority gate can operate as an AND or OR gate by setting an input to 0 or 1.It is expected that the utilization emerging nanotechnologies for approximate computing could significantly improve performance and reduce power consumption. Approximate arithmetic circuits based on CMOS technology have been extensively studied [6-8]; however, applying these approximate designs directly to ML based nanotechnologies would lead to inefficient circuits. Therefore, a ML based approximate design must be analyzed by considering the specific properties of ML.

PROPOSED MODEL

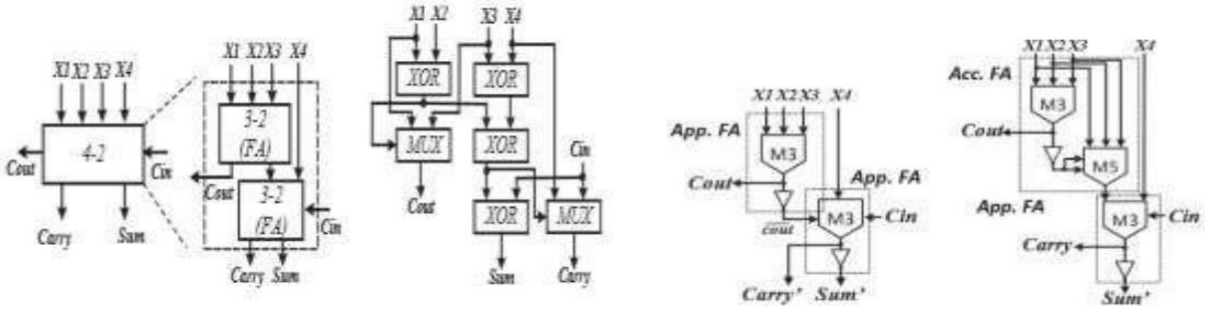

Fig2 Proposed Model

Design I

The gate level structure of the first proposed approximate4-2 compressor is depicted in Fig. 6a. As can be seen, only two approximate FAs (App. FA) are cascaded to realize such a low-complexity design.X1-X3inputs are assigned to the first App. FA andX4, Cin along with Cout are connected to the second App. FA. In this way, Cout can be obtained accurately for all input combinations using (5).Carry _is given in (6) with only 4 incorrect outputs as tabulated in Table IV. Sum' is accordingly derived in (7) by inverting the result of Carry ′with 12 incorrect output out of 32 possible outputs. Overall, Design I yields an error rate of 37.5% that is smaller than the error rate of employing the best approximate FA [38] and the same as that of the first design presented in [13]. Furthermore, Design I shows significant improvement for the critical delay (2Δ1) compared to the first approximate design in [13] (3Δ) and optimized design in [10] (3Δ)

$$Cout=M3(X1, X2, X3)$$

$$Carry'=M3\ (Cout, X4, Cin)$$

$$Sum'=Carry$$

Functionality Analysis

A full adder (FA) is one of the most frequently-used components in arithmetic circuitry. In addition to its regular use for addition, it is employed in other arithmetic operations such as subtraction, multiplication, and division. For instance, multiplication has been implemented using successive additions. Moreover, FA is the key component and optimization target of many DSP algorithms. Hence, in order to obtain a high performance DSP system, I need to design energy efficient and low complexity adder. While extensive work has been done in designing approximate adders, the project efforts on accuracy-configurable approximate adders are limited. Let A, Band Cin be inputs of an accurate full adder, the principle Boolean expression of Carry out (Cout) and accurate Sum (Sumacc) of FA cell are as follows:

Cout=AB+ACin+BCin=M3 (A, B, Cin)

Sumacc=ABCin+ $\bar{A}\bar{B}$Cin+ $\bar{A}$Bin+A $\bar{B}$ Cin(2)

Some Boolean expressions for Sumacc and Cout of FA based on inverters and MGs have been reported in. As can be seen in (1),Cout can be readily derived with a 3-input MG. Alternatively, Sumacc can be obtained by using 3-and 5-input MG functions as (3).

Inputs			Acc. Outputs		App. Outputs			
A	B	C_{in}	C_{out}	Sum	C_{out}		Sum	
0	0	0	0	0	0	✓	1	✘
0	0	1	0	1	0	✓	1	✓
0	1	0	0	1	0	✓	1	✓
0	1	1	1	0	1	✓	0	✓
1	0	0	0	1	0	✓	1	✓
1	0	1	1	0	1	✓	0	✓
1	1	0	1	0	1	✓	0	✓
1	1	1	1	1	1	✓	0	✘

Table 1 Truth Table

Sumacc=ABCin+AB.ACin.BCin) (A+B+Cin)

=ABCin+M3. (A+B+Cin)

=ABCin+M3.(A+B+Cin) +M3M3

=M5 (A, B, Cin, M3, M3)

=M5 (A, B, Cin, Cout, Cout) (3)

Table I shows the truth table of an FA. A close observation clarifies that six of eight outputs are correct if I make Sum=Cout. Based on this observation, I propose a stream-lined and cost-effective approximate FA circuit comprising one3-input MG and one cascaded inverter. The approximate Sum output (SumApp) of this adder is given by: SumApp=Cout=M3 (A, B, Cin)

Design II

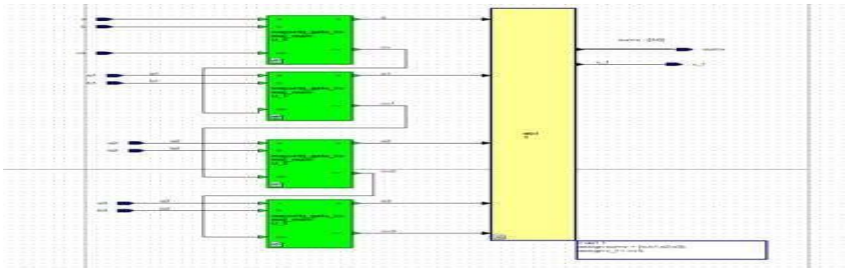

Fig 3 depicts the second proposed design employing one approximate

Fig. depicts the second proposed design employing one approximate FA (App. FA) and one accurate FA (Acc. FA) cell. Applying an accurate FA cell in the first level ensures that, in addition to Cout(5), Carry

output can be achieved correctly for all input combinations. This design generates 8 erroneous outputs for Sum′, therefore the error rate is now reduced to 25%. Asa trade-off between accuracy and circuit delay/complexity, design II incurs (3Δ) as the critical path delay with an additional 5-input MG compared to design I.

RESULTS:

FRONT END MULTIPLIER DESIGN PROCESS

Fig a MJT 4 Bit Gate Implementation

MULTIPLIER 16 BIT OUTPUT

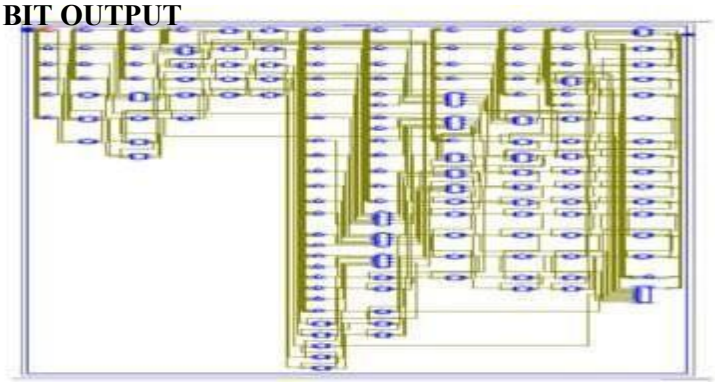

Fig b RTL schematic of the 16 bit multiplier

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	88	960	9%
Number of 4 input LUTs	155	1920	8%
Number of bonded IOBs	32	108	29%

Fig c Area utilization of the 16 bit MJT multiplier

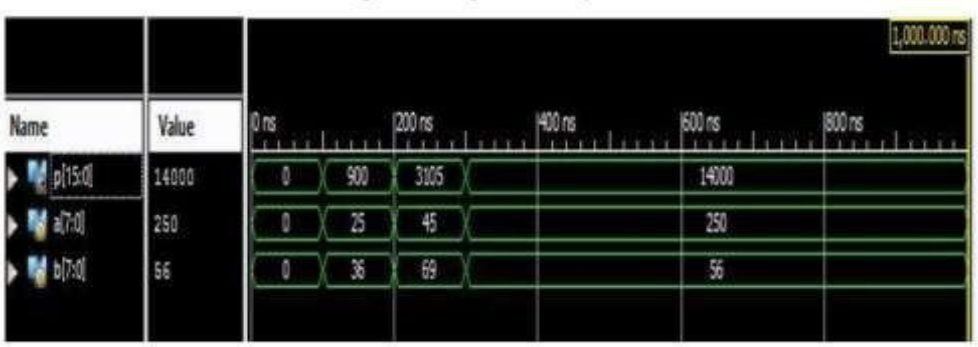

Fig d the output wave forms of the current design

SN0	Parameters	EXISTING	PROPOSED MJT
		4 bit MJT	
1	AREA	5.67um2	1.34 um2
2	Power	13.5 milli watts	64 microwatts
3	Delay	59ps	37ps

Table 6 Back-end Comparison table

Conclusion: My design implements a compact and energy-efficient accuracy-configurable adder design and two approximate 4:2, 3:2 compressors based on a composite spintronic device structure have been developed and assessed. Based on the majority logic, the proposed designs can be effectively utilized to trade off computation energy for more fluid levels output quality in DSP systems. A device-to-application simulation framework has been constructed and shown to be effective to evaluate the proposed hybrid spin-CMOS circuits.

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